

APM32F030xC

Errata Sheet

Version: V 2.1

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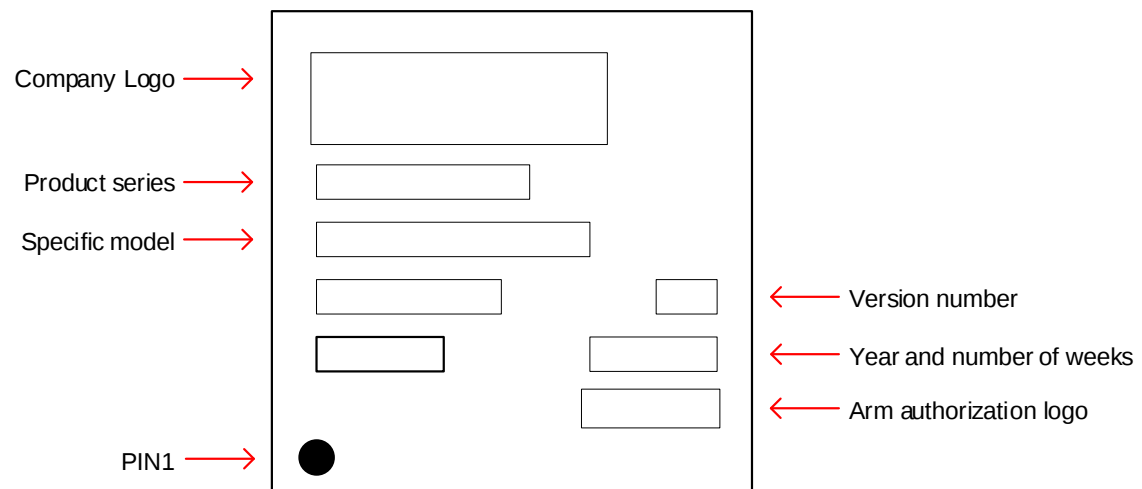
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1 Introduction

This Manual mainly introduces the limitations of the APM32F030xC series products during use. If you encounter the application scenarios described in the manual during the use of the product, please use the product according to the solutions provided in the manual; if no solution is provided, please avoid this application scenario.

2 Product Version and Silk Screen Printing Instructions

Figure 1 Product Version and Silk Screen Printing Instructions



3 Errata List

Table 1 Errata List

Category	Introduction	Product version	
		A4	B1
Clock	LSERDY flag bit	●	×
Flash	Flash low-temperature read	●	●
	Flash erase	●	●
	Flash wake-up	●	●
GPIO	I/O level	●	●

Note: "●" indicates that this errata description is involved in this version; the 'X' indicates that it is not involved in this version.

4 Clock

4.1 LSE RDY flag bit

Problem description

After the LSE clock is turned on normally, if the software turns off LSE, the LSE ready bit may not be cleared to zero.

Solutions

Choose either of the following solutions:

- Configure LSE_REDAY_CNT register to 00;
- Related problems can be solved by migrating the B1 version.

4.2 PLL frequency multiplication

Problem description

After doubling to 24MHz using PLL, the frequency output through the PA8 pin is unstable.

Solutions

Choose either of the following solutions:

- When using PLL multiplication, first use a large multiplication coefficient to increase the frequency of the VCO, and then output at a lower frequency. For example, increase the PLL frequency to 48MHz and then divide its frequency to 24MHz through an AHB prescaler.
- Related problems can be solved by migrating the B1 version.

5 Flash

5.1 Flash low-temperature read

Problem description

At low temperature ($\leq -35^{\circ}\text{C}$), there may be read errors during program download.

Solutions

Configure Flash_OP[19:20] to 11.

5.2 Flash erase

Problem description

Erasing the Flash without waiting for the FlashBUSY state to end will result in failure of the Flash chip erase.

Solutions

In FlashBUSY state, chip erase cannot be performed, and it can be performed only when the wait state is over.

5.3 Flash wake-up

Problem description

The low-power and AHB frequency division scenario may result in abnormal clearing of the dcode buffer, thus entering hardfault.

Solutions

In the scenarios of configuring through software in Flash page/chip erase, program or system low-power (e.g. stop) wakeup, the frequency of AHB is not divided.

6 GPIO

6.1 I/O level

Problem description

After GPIO is powered on, some individual I/O (PC13, PA5) may have abnormal level (the normal waveform is a 0V straight line), which can cause external NMOS mis-conduction.

Solutions

For individual I/O pins (PC13, PA5), abnormal level (e.g. process leakage) may occur, and the abnormal conditions can be avoided by improving the external hardware reliability design.

7 Revision history

Table2 Document Revision History

Date	Version	Revision History
August 2024	2.0	New edition
August 2025	2.1	(1) Add Chapter 4.2

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